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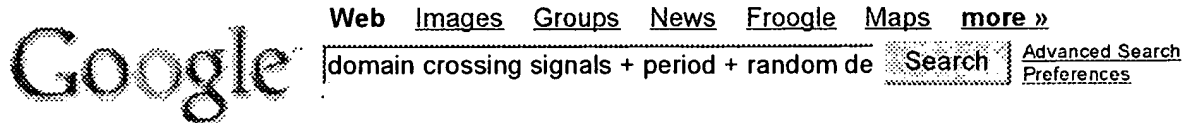
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<u>EETimes.com - Clock **domain** modeling is essential in high density ...</u>
All clock **domain crossing** logic should be contained in the bus adapter module. ...
naturally introduces a one or two receive clock **period delay**, ...
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Because the synchronizer imposes a two receive clock **delay** and because at ... **domain**
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<u>Semiconductor device for **domain crossing** - Patent 6980479</u>
a **domain crossing** sensing block in response to a operation mode **signal**, first and second
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clock **period**. Assume that. is the **delay** time of the ith. **delay** cell, ... PD, implemented by a
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<u>FPGA-FAQ 0017 Tell me about Metastability</u>
Since all flops are clocked by the same clock **signal**, all logic paths have the same
worstcase **delay** requirements, which is clock **period** minus **flipflop** ...
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<u>FPGA FAQ comp.arch.fpga archives - messages from 29675</u>
De-rate > the Tco of the **domain crossing** FFs by some multiple, say 6, of the unrouted >
delay. Then set up constraints like this: > > TIMESPEC TSSync = FROM ...
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of ... naturally introduces a one or two receive clock **period delay**, ...
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<u>Using **delay** - Patent Storm</u>
A method for distributing clocks to **flip-flop** circuits which constitute a logic ... The **signal**
phase shifting circuit includes a reference **signal period** ...
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channels with **random delay**, and. merge the channel outputs. sampler ...
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